(19) Japan Patent Office (JP)

(12) **KOKAI TOKKYO KOHO** (A)
[OFFICIAL GAZETTE FOR UNEXAMINED PATENT APPLICATIONS]

(11) Japanese Patent Application Kokai Publication Number: **H08-213605**

(43) Publication Date: August 20, Heisei 8 (1996)

(51) Int. Cl.[6]		Identification Code	JPO File No.	F I		
H 0 1 L	29/78					
	21/336					
	21/225	P		H 0 1 L	29/78	301 P

Examination Requested: Not yet requested
Number of Claims: 2 OL (5 pages in total) [Japanese text]

(21) Application Number: H07-17554
(22) Application Date: February 6, Heisei 7 (1995)
(71) Applicant: 000000295
Oki Electric Industry Co. Ltd. [Oki Denki Kogyo Kabushiki Kaisha]
7-12, Toranomon 1-chome, Minato-ku, Tokyo, Japan
(72) Inventor: Nishikawa Satoru
C/O Oki Electric Industry Co. Ltd.
7-12, Toranomon 1-chome, Minato-ku, Tokyo, Japan
(74) Agent: Funabashi Kuninori, patent attorney

(54) **TITLE OF THE INVENTION:**

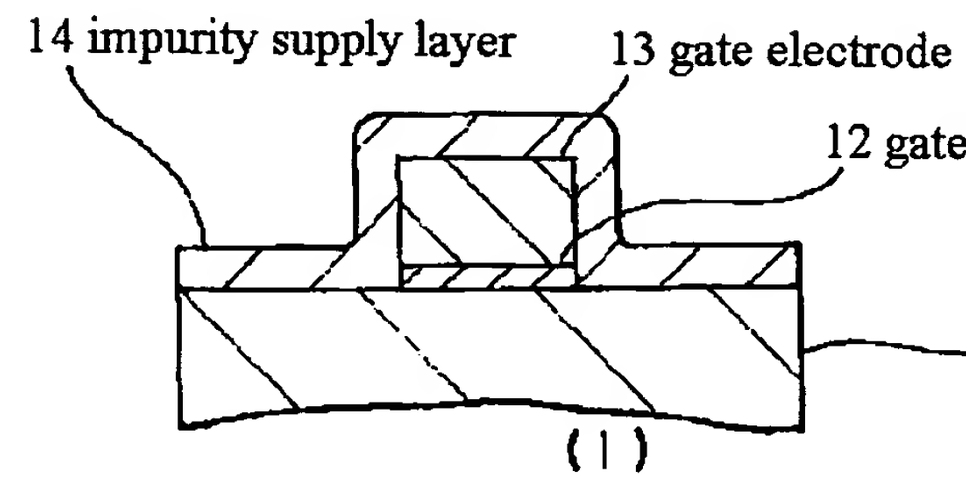
A method of manufacturing an MOS transistor

(57) **ABSTRACT**

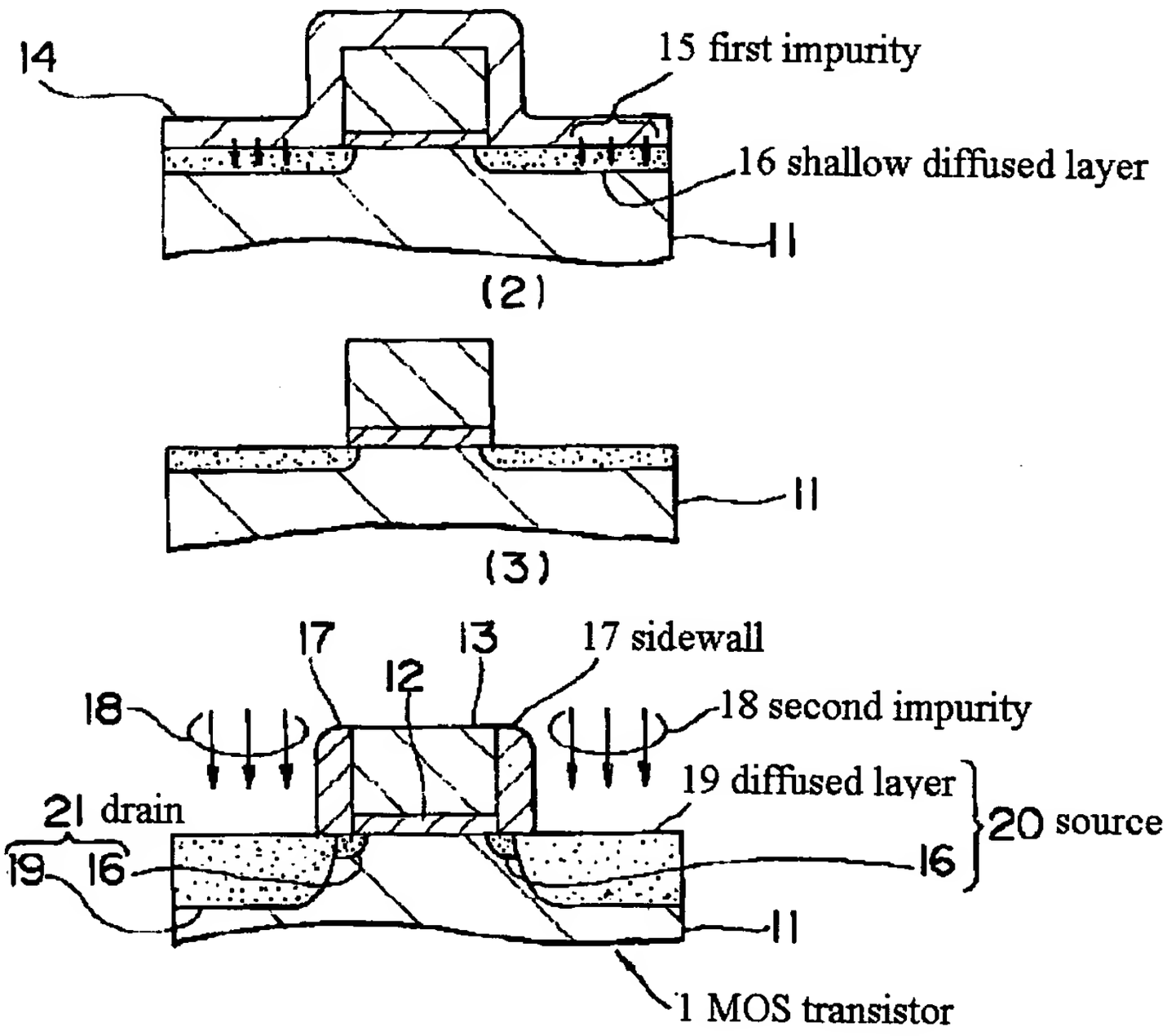
Purpose: To provide a method of manufacturing a MOS transistor having a shallow diffused layer containing high concentrations of impurities.

Constitution: A method of manufacturing an MOS transistor comprises four steps. In the first step, a first-impurity supply layer 14 of SiGe containing the first impurity is formed in a non-oxidizing environment on a substrate 11, whereon a gate electrode 13 has been formed through the intermediary of a gate insulating film 12. In the second step, a shallow diffused layer 16 for source and drain is formed by heat treatment, whereby the first impurity 15 undergoes solid-state diffusion by migrating from the impurity supply layer 14 into the substrate 11. In the third step, the impurity supply layer 14 is removed. In the fourth step, sidewalls 17 are first formed on the sides of the gate insulating film 12 and the gate electrode 13, and a diffused layer 19 for a source 20 and a drain 21 is then formed by ion implanting a second impurity 18 of the same

conductivity type as the first impurity 15 into the parts of the substrate 11 that are not covered by the sidewalls 17 or the gate electrode 13.



(1)



(2)

(3)

CLAIMS

What is claimed is:

1. A method of manufacturing an MOS transistor, comprising:

a first step for forming a gate electrode through the intermediary of a gate insulating film on a silicon substrate and then for forming, in a non-oxidizing environment, an impurity supply layer, which is made of silicon-germanium or germanium and contains a first impurity, on the exposed surface of the substrate;

a second step for forming a shallow diffused layer for source and drain using heat treatment, whereby the first impurity is made to undergo solid-state diffusion from the impurity supply layer into the substrate;

a third step for removing the impurity supply layer; and

a fourth step for forming, after sidewalls are formed on the sides of the gate insulating film and the gate electrode, a diffused layer section for source and drain by ion implanting a second impurity of the same conductivity type as the first impurity into the parts of the substrate that are not covered by the sidewalls or the gate electrode.

2. A method of manufacturing an MOS transistor according to claim 1, wherein:

the composition of the impurity supply layer is $Si_{1-x}Ge_x$, where x = 0.2–1; and

a mixed solution of fluoric acid and nitric acid is used in the third step as an etching solution for removing the impurity supply layer by wet-etching.

DETAILED DESCRIPTION OF THE INVENTION

[0001]
[Field of the Invention] The present invention relates to a method of manufacturing an MOS transistor.

[0002]
[Prior Art] MOS transistors having a shallow junction for the source and drain are fabricated according to a method described on pages 2,264–2,271 of *IEEE TRANSACTIONS ON ELECTRON DEVICES**, **40** [12] (1993) (US), in the following manner. Sidewalls, which are

---

* Translator's note: A typographical error in the original text assumed.

made of oxidized silicon (boron*-doped silicate glass (BSG)), are formed on the sidewalls of a gate insulating film and a gate electrode, both of which are formed on a silicon substrate. The boron in the BSG sidewalls is made to undergo solid-state diffusion into the substrate, to form a shallow diffused layer section for source and drain. Next, boron is introduced into the substrate from above the sidewalls by ion implantation to form a diffused layer section for source and drain.

[0003] With the above method of manufacturing an MOS transistor, the shallow diffused layer is formed on the surface layer, the depth of which is in the order of 40 nm, of the substrate with a peak [boron] concentration in the order of $10^{19}/cm^3$ as a result of the migration of boron from the BSG, which constitutes the sidewalls, by solid-state diffusion, to form the MOS transistor having the shallow source and drain junction. In recent years, as semiconductor devices are becoming further integrated and offering improved performance, the micro-miniaturization of the element structure is underway. Moreover, in order to further advance the miniaturization of the above-described MOS transistor, it is necessary to form the source and the drain having a shallow junction with a low resistance by way of increasing the concentration of the impurities in the shallow diffused layer, in order to prevent the short-channel effect and improve the current driving capacity of the miniaturized MOS transistor.

[0004]
[Problems to be Solved by the Invention] However, the above-described method of manufacturing an MOS transistor has posed some problems. In other words, it is known that the impurity becomes segregated in between oxidized silicon and silicon. For this reason, boron becomes segregated in the interface between the silicon substrate and the BSG sidewalls during the solid-phase diffusion, with a result that the concentration of boron in the substrate can reach only about one tenth of that in the sidewalls. Consequently, it is impossible to obtain a shallow diffused layer containing a high concentration of the impurity using the above-mentioned method for manufacturing an MOS transistor.

[0005] Moreover, there is no model that can accurately predict the segregation phenomenon of the impurity in the interface between silicon and oxidized silicon. Consequently, in order to be able to form a shallow diffused layer of a desired thickness and concentration using the above-described solid-state diffusion, a number of separate experiments must be carried out before the conditions of heat treatment could be determined. Furthermore, the step for forming the BSG on the substrate is carried out in an oxidizing environment. For this reason, the substrate sometimes becomes oxidized during the formation of the BSG film constituting the sidewalls, and this causes an oxide film to be formed on its surface. Moreover, the quantity of the impurity diffused from the sidewalls into the substrate varies greatly depending upon whether or not the oxide film is present in between the substrate and the sidewalls. However, it is extremely difficult to control the thickness of the above oxide film. Moreover, it is also extremely difficult to determine whether the oxide film is present on the bottom of the sidewalls.

[0006] For these reasons, it is impossible to obtain shallow diffused layers of a desired depth and concentration by controlling the diffusion of boron from the sidewalls into the substrate using the above-described method of manufacturing an MOS transistor.

[0007]
[Means for Solving the Problems] The method of manufacturing the MOS transistor of the present invention follows the steps outlined hereinafter in order to overcome the problems described above. Firstly, in the first step, an impurity supply layer comprising silicon-germanium or germanium and containing a first impurity is formed on a substrate, whereon a gate electrode has been formed through the intermediary of a gate insulating film. This impurity supply layer is formed under a non-oxidizing environment. This is followed by the second step, wherein a shallow diffused layer section for the source and drain is formed. This is done using heat treatment in order to cause the solid-state diffusion of the first impurity from the impurity supply layer into the substrate. This is followed by the third step, wherein the impurity supply layer is removed. During the fourth step, after sidewalls are formed on the sides of the gate insulating layer and the gate electrode, a second impurity, which is of the same conductivity type as the first impurity, is ion implanted into the parts of the substrate that are not covered by the sidewalls or the gate electrode, to form a diffused layer section for the source and drain.

[0008]
[Operation] With this method of manufacturing an MOS transistor, because the impurity supply layer of silicon-germanium or germanium is formed on the silicon substrate in a non-oxidizing environment, the impurity supply layer is formed on the substrate without oxidizing its surface. Because the first impurity is made to undergo solid-state diffusion from the impurity diffused* [sic] layer into the substrate, the first impurity is diffused into the substrate without becoming segregated in the interface between the impurity supply layer and the substrate. Moreover, the diffusion constant of the fist impurity diffused into the substrate is about the same as that in the impurity supply layer.

[0009]
[Preferred Embodiments] An embodiment of the present invention will be described hereinafter with reference to the steps illustrated in the accompanying diagram, Fig. 1. Firstly, during the first step shown in Fig. 1(1), a gate electrode 13 is pattern formed on a substrate 11, which has been isolated by a field oxide film, not shown in the diagram, through the intermediary of a gate insulating film 12. Here, the oxide film is formed on the substrate 11, which is made of silicon, and then a polysilicon film is formed thereon. Phosphate is then introduced into the polysilicon film using $POCl_3$ as a diffusion source. A resist pattern is then formed on the polysilicon film by lithography, and the appropriate parts of the polysilicon film and the oxide film are etched using the resulting resist pattern as a mask. This results in the formation of a gate insulating film 12, which is comprised of the oxide film, and a gate electrode

---

* Translator's note: Probably "impurity supply layer" is intended.

13, which is made of n-type silicon. Incidentally, p-type polysilicon, polycide, or metals such as tungsten may be used as the material for the gate electrode 13.

[0010] Next, in cases wherein there is a possibility that the surface of the substrate 11 is covered by a natural oxide film, it is removed by etching using a weak fluoric acid solution. Then, an impurity supply layer 14, which consists of silicon-germanium (hereinafter referred to as "SiGe") or germanium and contains a first impurity, is formed on the substrate 11 in a manner so as to cover the gate insulating film 12 and the gate electrode 13. Here, boron of the p-type conductivity is used for the first impurity. The substrate 11 is then put into a low-pressure chemical vapor deposition (CVD) furnace while care is taken to prevent its surface from being oxidized. Then, the impurity supply layer 14 is formed on the substrate 11 under a non-oxidizing environment in the low-pressure CVD furnace using SH_4, or SH_2Cl_2, GeH_4 and B_2H_6 as the material for the gas.

[0011] The composition of the SiGe constituting the impurity supply layer 14 is $Si_{1-x}Ge_x$, where $x = 0.2$ to 1, and is set in a manner so as to offer an [appropriate] etching selectivity between the substrate 11 and the impurity supply layer 14. Moreover, the thickness of the impurity supply layer 14 is set in the range of several nm to 100 nm, optimally about 10 nm, so that it can be removed readily in the subsequent step. The concentration of the first impurity in the impurity supply layer 14 is set at around $10^{20}/cm^3$.

[0012] In the second step shown in Fig. 1(2) that follows, the first impurity 15 in the impurity supply layer 14 is subjected to undergo solid-state diffusion into the silicon substrate 11 to form a shallow diffused layer 16 in the substrate 11. According to what appears on pages 5,520–5,526 of the *J. Appl. Phys*, **74** [9] (1993-11-1), boron used as the first impurity 15 between SiGe and Si does not become segregated. Therefore, the impurity 15 present in the impurity supply layer 14 is diffused sufficiently into the substrate 11 in the solid-state diffusion by heat treatment. Moreover, the diffusion constant of boron in Si is nearly the same as that of boron in SiGe. For this reason, it is possible to predict the thickness and the [impurity] concentration of the shallow diffused layer 16, which is formed in the surface layer of the substrate 11, by performing a commonly used process simulation, if the diffusion constant in the impurity supply layer 14 is determined in advance.

[0013] Consequently, the temperature, the duration and other conditions of heat treatment are selected here according to the [impurity] concentration and the thickness of the shallow diffused layer 16. For instance, when the concentration of the first impurity 15 in the impurity supply layer 14 is $10^{20}/cm^3$ and the shallow diffused layer 16 is to be formed in the surface area of the substrate 11 to a depth of 40 nm with an [impurity] concentration of $10^{19}/cm^3$, heat treatment is carried out at 850°C for 30 minutes.

[0014] This is followed by the third step, shown in Fig. 1(3), where the impurity supply layer 14 is removed from the top of the substrate 11. Here, the impurity supply layer 14 is removed by wet-etching using a mixture of nitric acid and fluoric acid solutions as the etching

solution while ensuring the etching selectivity between the impurity supply layer 14 and the substrate 11.

[0015] According to pages 2,943–2,947 of the *J Electrochem. Soc.*, **139** [10] (1992) (US), for example, the etching rate of Si is 0.4 nm/min using an etching solution containing the mixture HNO_3 : HF (0.5% aqueous solution) : H_2O = 35 : 10 : 20, whereas the etching rate of $Si_{0.7}Ge_{0.3}$ is 41 nm/min, giving a selectivity of about 10. Moreover, because the etching rate of oxidized silicon using the above etchant is low, the etching of the above-mentioned field oxide film can be ignored.

[0016] After the impurity supply layer 14 is removed in the manner described above, step 4, described in Fig. 1(4), is carried out. Here, sidewalls 17 of oxidized silicon are first formed on the sidewalls of the gate electrode 13 and the gate insulating film 12. A second impurity 18 is then ion implanted from the exposed surface of the substrate 11 not covered by the gate electrode 13, the gate insulating film 12 and the sidewalls 17. The second impurity 18 should be of the same conductivity type as the first impurity (15), and boron, which is what was used as the first impurity, is employed here as the second impurity 18. The substrate 11 is then ion implanted with BF_2^+, which contains boron, and the diffused layer 19 is formed by diffusing the second impurity 18 into the substrate 11 by applying activation heat treatment. In this manner, an MOS transistor 1 furnished with a source 20 and a drain 21 both having the shallow diffused layer 16 is fabricated.

[0017] In the embodiment described above, the impurity supply layer 14 of SiGe was formed on the substrate 11 after the natural oxide film forming the surface layer had been removed from the substrate 11. In this case, the impurity supply layer 14 is monocrystalline. When the natural oxide film is left on the surface of the substrate 11, however, the impurity supply layer 14 is polycrystalline. Consequently, it is possible to determine whether the natural oxide film remains between the substrate 11 and the impurity supply layer 14 during the manufacturing process of the MOS transistor by analyzing the impurity supply layer 14 using methods such as x-ray diffraction or electron diffraction in order to find out its crystalline structure. As a result, it becomes possible to conduct a non-destructive test for the inadequacy of the diffusion of the impurity remaining in the natural oxide film.

[0018] Moreover, in the embodiment described above, the impurity supply layer 14, which becomes the source of impurity supply for the shallow diffused layer 16, is removed from the top of the substrate 11 after the heat treatment of the second step. For this reason, in dealing with the diffusion of the impurity in the shallow diffused layer 16 when carrying out activation heat treatment of the diffused layer 19, for example, diffusion within the substrate 11 only needs to be taken into consideration.

[0019] Moreover, when germanium containing the first impurity 15 is used for the impurity supply layer 14 in the above embodiment, the impurity supply layer 14 is formed on the substrate 11 without oxidizing the latter's surface, as was the case in the above embodiment, thus allowing the first impurity to be diffused sufficiently into the substrate 11. As well, this allows

for the removal of the impurity diffused layer 19 from the surface of the substrate 11 while maintaining the selectivity with respect to the substrate 11, which is comprised of Si.

[0020] Incidentally, the above embodiment was described using the example of manufacturing a p-MOS transistor. Nevertheless, the present invention is also applicable to n-MOS transistors. In that case, n-type impurities such as phosphorus (P) or arsenic (As) should be used as the first impurity contained in the impurity supply layer 14 and as the second impurity. This allows for the formation of an MOS transistor having a shallow diffused layer similar to that of the embodiment described above.

[0021]
[Advantages of the Invention] As described above, the method of manufacturing an MOS transistor of the present invention involves forming the impurity supply layer, which is to serve as the supply source for solid-state diffusion and is comprised of silicon-germanium or germanium, on the substrate in an non-oxidizing environment, without causing the formation of an oxide film on its interface with the substrate. Consequently, the first impurity can be diffused into the substrate without becoming segregated in the interface between the impurity supply layer and the substrate. As a result, a shallow diffused layer containing a high concentration of the impurity can be formed in the surface layer of the substrate of the MOS transistor. Consequently, a miniaturized MOS transistor can be designed in a manner so as to prevent the short channel effect and to improve its current driving capacity. Moreover, because the impurity in the impurity supply source has nearly the same diffusion constant as that of the impurity in the substrate, simulations of the depth and the [impurity] concentration of the shallow diffused layer can be readily performed, thus making it possible to obtain the shallow diffused layer of a desired depth and [impurity] concentration for the miniaturized MOS transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram illustrating steps according to an embodiment of the present invention.

Description of the Reference Numerals

11: substrate
12: gate insulating film
13: gate electrode
14: impurity supply layer
15: first impurity
16: shallow diffused layer
17: sidewall
18: second impurity
19: diffused layer
20: source
21: drain

【図１】

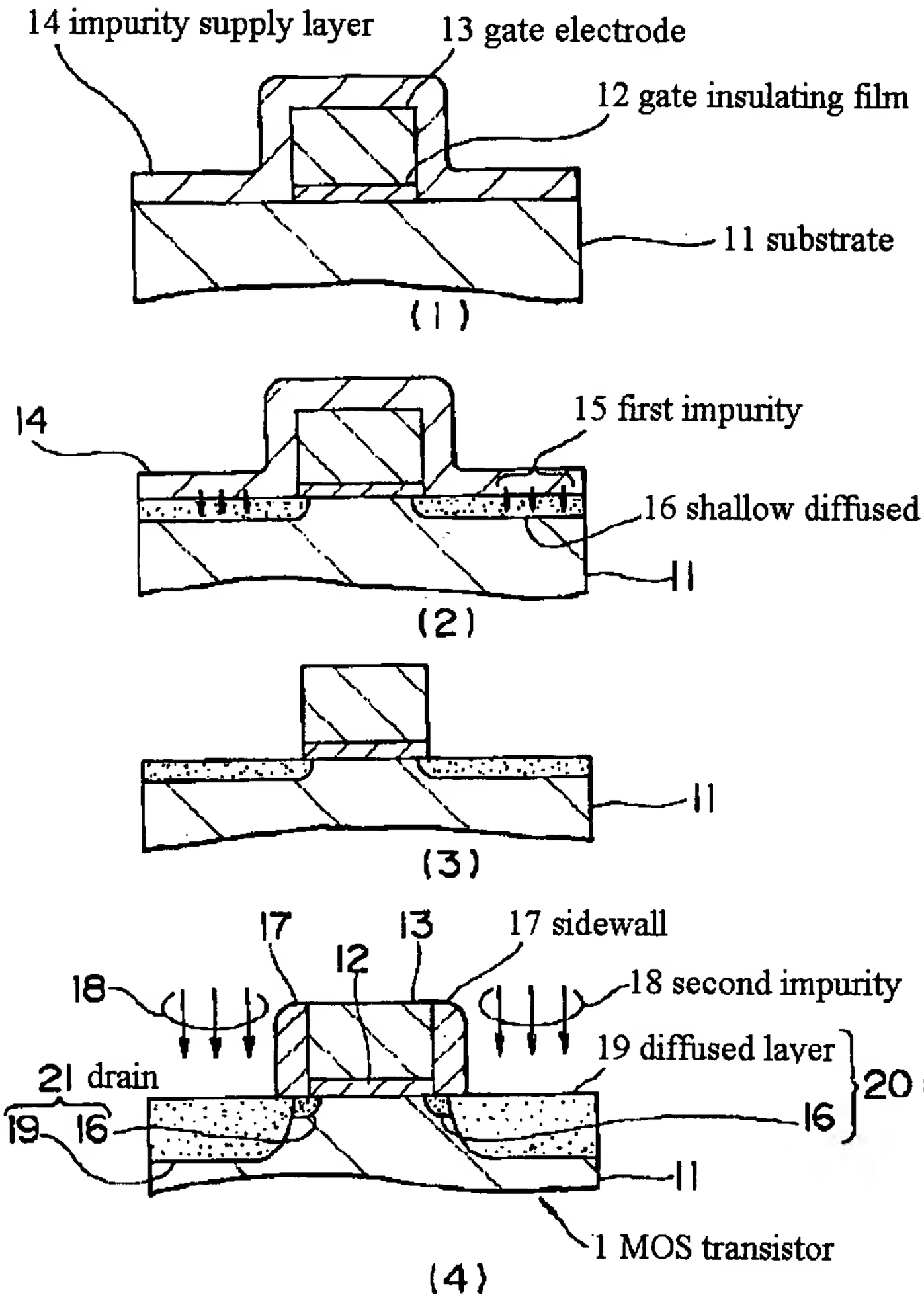


Diagram illustrating the steps according to an embodiment of the present invention